CBCS Scheme

USN | | | | | | | | | | |

15EE35

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. With basic block diagram, explain the combinational logic circuit. **(04 Marks)**

b. Reduce the following function using K-map technique and implement using basic gates

i) $f(P, Q, R, S) = \sum m(0, 1, 4, 8, 9, 10) + d(2, 11)$

ii) $f(A, B, C, D) = \pi M(0, 2, 4, 10, 11, 14, 15)$ **(12 Marks)**

OR

2 a. Simplify using the Quine-Mccluskey minimization technique.
$Y = f(a, b, c, d) = \sum m(0, 2, 8, 10)$ **(08 Marks)**

b. Simplify the given function using MEV technique.
$f(a, b, c, d) = \sum(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$. **(08 Marks)**

Module-2

3 a. With the aid of general structure, clearly distinguish between a decoder and encoder. **(05 Marks)**

b. Implement following multiple output function using one 74LS138 and external gates.
$F_1(A, B, C) = \sum m(1, 4, 5, 7)$
$F_2(A, B, C) = \pi M(2, 3, 6, 7)$ **(06 Marks)**

c. Draw the interfacing diagram of ten keypad interface to a digital system using decimal to BCD encoder (IC 74LS147: Decimal to BCD priority encoder). **(05 Marks)**

OR

4 a. Design a full adder by constructing the truth table and simplify the output equations. **(06 Marks)**

b. Write a truth table for two-bit magnitude comparator. Write the Karnaugh map for each output of two bit magnitude comparator and the resulting equation. **(10 Marks)**

Module-3

5 a. What is the difference between a flip-flop and a latch? With logic diagram and truth table, explain the operation of gated SR latch. **(08 Marks)**

b. Explain the operation of Master slave JK Flip-flop along with its circuit diagram. **(08 Marks)**

OR

6 a. Explain the working principle of four bit binary ripple counter, with the help of a logic diagram, timing diagram and counting sequence. **(10 Marks)**

b. With logic diagram and counting sequence explain Mod – 4 ring counters. **(06 Marks)**

Module-4

7 a. Distinguish between Moore and Mealy model with necessary block diagrams. **(08 Marks)**

b. Give output function, transition table and state diagram by analyzing the sequential circu shown in Fig. Q7(b). **(08 Marks)**

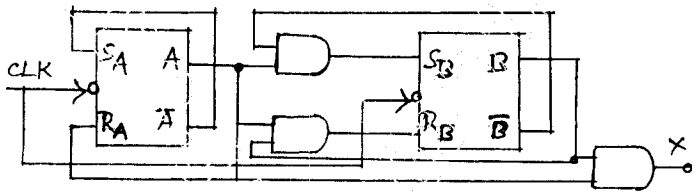

Fig. Q7(b)

OR

8 a. Write the basic recommended steps for the design of a clocked synchronous sequenti circuit. **(06 Marks)**

b. Design a synchronous counter using J-K flip flops to count the sequence 0, 1, 2, 4, 5, 6, 0, 2. Use state diagram and state table. **(10 Marks)**

Module-5

9 a. Explain brief history of HDL and structure of HDL module. **(06 Marks)**

b. List the classification of VHDL data types. Compare the VHDL data types and Verilog dat types. **(10 Marks)**

OR

10 a. Explain signal declaration and signal assignment statements with relevant example. **(06 Marks)**

b. Write a data flow description VHDL for a system that has three 1-bit inputs a (1), a(2) an a(3) one 1-bit output b. The least significant bit is a(1) ; and b is 1, only when (a(1) a(a(3)) = 1, 3, 6 or 7 (all in decimal) otherwise b is 0. Derive a minimized Boolean function the system and write the data flow description. **(10 Marks)**

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